Abstract

A method of designing a custom circuit device begins with a high level architecture of subsystems coupled by virtual wires. The method comprises first through third steps. The first step comprises spatially placing the subsystems onto tiles. The second step comprises routing the virtual wires that cross boundaries of the tiles onto an interconnect architecture. The interconnect architecture comprises switches and registers. Some of the switches route a signal from a first subsystem located on a first tile to a second subsystem located on a second tile. At least two of the registers consecutively latch the signal at a time interval of no more than a repeating time period. The third step comprises scheduling of tasks according to clock cycles. According to an embodiment of the method, the repeating time period comprises a clock cycle period. According to another embodiment of the method, the repeating time period comprises a multiple of the clock cycle period.